The Examiner stated on page 3 of the Office Action that with respect to the Nagai reference, "the lower electrode (20) of the upper capacitor could also have been formed simultaneously with the formation of the storage node (25) of the cell capacitor and would have been obvious to one of ordinary skill in the art at the time of the invention to provide more efficient processing." The Examiner cited no specific portion of the art for this contention. Thus, the Examiner appears to concede that the art does not expressly describe "simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element" as recited in claim 1. The rational given by the Examiner for the modification of Nagai was ". . . to provide better processing." However, as described below, the Examiner cited no specific portion of the art that establishes that such a modification would result in more efficient processing. Moreover, the Examiner cited no portion of the art that establishes that the proposed modification would be desirable or successful.

Applicant notes that as described in Nagai at col. 15, lines 6-11, if the Examiner considers the reference number 20 in Nagai (which includes layers 18 and 19) as a lower electrode of a capacitor element in a peripheral area, then such electrode 20 is described as being formed at the same time as layers 18 and 19 of bit line 21 in the memory cell area. Thus, because Nagai already forms the electrode 20 simultaneously with the bit line layers 18 and 19, there is no reason why one of ordinary skill would seek to alter the method of Nagai to form the lower electrode at a later time in the process (at the time the storage node 25 is formed) as suggested by the Examiner because no net reduction in steps would occur. Moreover, Nagai forms the electrode 20 from layers of polysilicon 18 and tungsten silicide 19. Nagai forms the storage node 25 in the memory cell region from polysilicon. Thus, the combination proposed by the Examiner would also appear to change the electrode from layers of polysilicon and tungsten silicide to one layer of polysilicon. Moreover, the combination proposed by the Examiner would require a significant modification in the steps of the Nagai method, in which, as seen in Nagai at Figs. 5-15, forms the electrode 20 of a capacitor in the peripheral area together with the bit line 21 of the capacitor in the memory cell area (Nagai Figs 11-12), then later forms the storage nodes 25, 26 of the memory cell capacitor (Nagai Figs. 13-14). Modifying Nagai to form the capacitor electrode 20 of a capacitor in the peripheral area at the same time as storage nodes 25, 26 would require a considerable change in many of the Nagai process steps. The Examiner does not appear to have

established that one of ordinary skill would reasonably be able to make the combination proposed by the Examiner without having to significantly change the Nagai process, or that any particular benefit would result.

Accordingly, for at least the above reasons, applicant respectfully submits that the Examiner has provided no legally sufficient basis for the suggested modification of the cited art, and accordingly, the rejection of claim 1 should be withdrawn. The rejection of claim 15 should be withdrawn for at least similar reasons as explained above for claim 1.

Regarding claim 17, the Examiner conceded at page 3 that "Nagai does not disclose connection at the bottom surface of the lower electrode, but rather at the top surface of the upper electrode." The Examiner then stated that "it has been ruled that where functional equivalence is maintained, rearranging parts of an invention involved only routine skill in the art," citing In re Japikse 86 USPQ 70. The Examiner cited Nagai at col. 13, lines 44-54 for am "embedded connection layer" with "one end connected to the impurity region and another to the surface of the capacitor". Applicant notes that while Nagai states at col. 13, lines 43-46, that the "major surface of the semiconductor substrate 1 and the second electrode 20 are connected with each other through the openings 37 and 38," the Examiner cited no Figures of Nagai that appear to show how the connection is made. As seen in Fig. 17, for example, the openings 37 and 38 do not appear to extend to the electrode 20.

Applicant also notes that in the In re Japikse case (86 USPQ 70 (CCPA 1950)), the concept cited by the Examiner appears to have related to an apparatus claim in a mechanical device (hydraulic press), and related to the position of a switch. The court found no error in the holding that "there would be no invention in shifting the starting switch disposed by Cannon to a different position since the operation of the device would not thereby be modified." 86 USPQ at 73. However, claim 17 in the present case is not an apparatus claim, but is a method claim. The claimed method would have to be substantially modified to following the suggestion of the Examiner. The proposed modifications, which include forming openings 37, 38, through a large number of layers (both lower than and above the capacitor 20), positioned a distance away from the capacitor 20, and then contacting the capacitor upper electrode layer, entails substantial changes to the claimed method in both the number of steps necessary and the timing of the steps. Such changes would substantially alter the method. The Examiner cited no portion of the art that

suggests the desirability of such changes, and indeed it appears that such changes would add steps to the process and result in a less compact structure, and thus would not be desired. The Examiner does not appear to have provided any sufficient motivation for the proposed modification, as required under current legal standards. Accordingly, for at least the above reasons, applicant respectfully submits that the rejection of claim 17 should be withdrawn.

The rejection of dependent claims 18 and 23-29 should be withdrawn for at least similar reasons as claim 17. Applicant also notes that claim 29 can be further distinguished in a manner similar to that described above for claim 1.

Claims 2-4 and 19-22 were rejected under 35 U.S.C. 103(a) as unpatentable over Nagai in view of Choi et al. (US 6,040,596). The rejection is respectfully traversed. Claims 2-4 depend from claim 1 and can be distinguished at least in a similar manner as claim 1. Claims 19-22 depend from claim 17 and can be distinguished at least in a similar manner as claim 17. Moreover, applicant respectfully submits that the Examiner's citation to Choi does not support the Examiner's proposed modification to Nagai. Choi at col. 5, lines 62-65, states "[n]ow that the sheet resistance of the resistor 102 is varied depending on the impurity concentration of the polysilicon, the size may be changed based on the impurity concentration of the doped polysilicon." This statement appears to mean that depending on the impurity concentration of the doped polysilicon used for the plate electrode 38, the size of the resistor 102 may be varied to obtain the desired resistance. The Examiner cited no portion of the art that suggests that Choi would motivate one of ordinary skill to vary the process so that "a resistance value of the first resistance element is lower than a resistance value of the second resistance element" as recited in claim 2, for example. At best, it appears that such a combination would result in resistance elements having the same resistance value. Accordingly, applicant respectfully submits that for at least the additional reasons described above, the rejection of claim 2 should be withdrawn. Claims 3 and 19-20 can be similarly distinguished. Regarding claims 4 and 21-22, applicant respectfully submits that the Examiner cited no portion of the art that would motivate one of ordinary skill to vary the resistance of only one resistance element by deploying a polycide. Accordingly, for at least this additional reason, the rejection of claims 4 and 21-22 should be withdrawn.

Accordingly, for at least the above reasons, applicant respectfully submits that the Examiner's citations to the art fail to establish a prima facie case of obviousness. Accordingly, the rejections of claims 1-4 and 15-29 should be withdrawn.

The Office Action also included various comments concerning the art and the non-patentability of features in various of the above mentioned claims. Applicant respectfully disagrees with the Examiner's non-patentability conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of this response.

Applicant respectfully submits that claims 1-4 and 15-29 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES VICTOR & MANN, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212
Customer No. 24033

Dated: May 28, 2003

tele general: (310) 556-7983
tele direct: (310) 871-8448
facsimile: (310) 556-7984

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 28, 2003.

Alan S. Raynes — May 28, 2003

Alan S. Raynes **(Date)**